

SHOP-FLOOR CONTROL FOR BATCH OPERATIONS WITH TIME CONSTRAINTS IN WAFER FABRICATION

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In wafer fabrications, engineers will set a queue time limit between particular operations to ensure the final product yield, which is named "time constraint." Due to the dilemma of increasing machine efficiency or decreasing the queue time of WIP, time constraint issues become more complex in batch processing. This work proposed a shop-floor control policy in serial-batch-serial processes with time constraints. The concept of safety stock ([S,s] policy) is introduced to control the WIP level, simultaneously avoiding machine idle and wafers exceeding time constraints. Length of time constraints, MTTR of machines and service rate of workstations are adopted to determine the batch size and boundaries of the WIP level. The job hold/release policy is addressed to control situations of excessively high WIP levels. Furthermore, the performances of the proposed model are compared with DJAH and MBSX rules. The results indicate that the proposed model could control the batch processing with time constraints more effectively.

Keywords: time constraints, wafer fabrications, batch processing, shop floor control, batch size

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1. INTRODUCTION

A time constraint (TC) is a time window set between two specific operations to prevent undesirable copper film oxidation or fluorine precipitation on wafer surfaces (Robinson and Giglio 1999, Tu and Liou 2006). Wafers have to be reworked or scrapped if TC is exceeded, which increases cycle time and decreases productivity. Effectively controlling workstations with TCs thus becomes an essential task for the semiconductor industry. However, as a result of high production volume, expensive equipment, and time consuming processes, machines used in wafer fabrication are usually required to operate at a high utilization level. Indeed, extremely high utilization of workstations causes difficulty in resolving TC issues.

The TC issues were first addressed between wet etch and furnace operations. Wafers have to start furnace operation within TC once they finish the wet etch process, otherwise they will be sent back to the wet etch workstation and reworked. In this stage, however, long batch accumulation and processing time will increase management difficulty. Machine efficiency and required time for batch formation become trade-off issues when determining the batch size. Low machine efficiency or long batch formation time will increase both the waiting time and the rate of exceeding TC (Rulken et al. 1998). Determining the batch size more precisely will be crucial for conquering TC issues in this stage.

There are many studies related to batch size determination in wafer fabrications (Fowler et al. 1992, Glassry and Weng 1991, Weng and Leachmen 1993). These studies have attempted to optimize the performances of batch-processing workstations by, for instance, maximizing throughput and minimizing cycle time. However, there was also a TC set following the furnace operation. Optimizing the output of the furnace workstation may increase the rate of wafers exceeding TC in the succeeding operation (Tu and Chen 2006). In some situations the batch size should be decreased, even if it results in lower machine efficiency, to prevent wafers from exceeding TC at the succeeding workstation. In batch size determination, therefore, the situations of the furnace operation should be considered simultaneously with those of the succeeding workstation.

Furthermore, the WIP could be held at the wet etch workstation (i.e. the operation without setting TC) to control the WIP levels in front of both the furnace and the succeeding workstations. Wolfgang and Joerg (2000) indicated that controlling the WIP level is crucial for conquering the issue of TC. Hence, drastic situations could be resolved by the job hold/release policies of the wet etch workstation, whereas they could not be settled by batch size adjustment (e.g. when the WIP levels of both the furnace and succeeding workstations are exceeding a safe level). By managing wafers released into this stage, the rate of exceeding TC and the incidence of machine idle, at both the furnace and succeeding operations, could be controlled simultaneously.

Accordingly, the purpose of this work is to develop a shop-floor control policy that resolves TC issues between the furnace workstation and its preceding and succeeding operations. The proposed model determines the batch size of the furnace operation dynamically by considering TC interval and WIP level. Furthermore, a job hold/release policy is involved in the proposed model in order to control the WIP at a safe level by adopting the safety stock $([S,s])$ concept. The goal of setting a safety stock level is not only to prevent wafers from exceeding TC, but also to reduce the probability of machine idle. Finally, the performance of the proposed model is compared with previous methodologies.

2. LITERATURE REVIEW

Previous studies related to batch size determination and shop-floor control rule in batch processes of wafer fabrications are reviewed in this section. The common methodology for determining batch size can be classified into two categories, Minimum Batch Size rule (MBS) and Look-ahead strategy. MBS, also called threshold policy, determines the batch size based on mean arrival rate and service rate of a workstation, but does not consider future customers' arrival information (Neuts, 1967, Deb and Serfozo 1973, Rulken et al. 1998). With the MBS rule, machines start operation while the batch size is greater than the threshold, otherwise they will wait for batch formation. Weng and Leachmen (1993) introduced multi-product into MBS and proposed the MBSX rule. In this policy, the customer with the longest waiting time will have the highest priority in the queue.

The look-ahead strategy was first addressed by Glassey and Weng (1991). They proposed the Dynamic Batch Heuristic (DBH) model with a time horizon, and took future arrival information into consideration in order to determine batch size dynamically. In this study, they presented evidence that proves DBH can perform better than the MBS rule. Fowler et al. (1992) introduced the concept of a rolling horizon into DBH and proposed the Next Arrival Control Heuristic (NACH) policy. NACH emphasized that the start of operation should be decided with every customer arrival and departure. Van Der Zee et al. (1997) introduced multi-product and multi-server into NACH and proposed the Dynamic Job Assignment Heuristic (DJAH). This study indicated that the system should minimize the cost per batch instead of the cost per unit time. MBSX and DJAH are methodologies which are commonly used for batch size

determination in furnace operations management. However, neither of these methods consider TC issues.

Except for the objective of optimizing the achievement of a batch-processing workstation, some studies focused on the performance of products. Cheraghi et al. (2003) proposed a Hybrid Genetic Algorithm (HGA) model to schedule the batch-processing machine to minimize the cycle time of the products. This work modified and relaxed some assumptions of the scheduling procedure proposed by Ikura and Gimple in 1986. However, only the issues with single batch-processing machines were considered in this study. Moreover, in such a complicated environment as wafer fabrication, a scheduling algorithm will be too complex to implement.

To address the complex issues of dispatching rules in wafer foundries, Wu and Hung (2008) proposed an enhanced Line Balance Starvation Avoidance (LBSA) algorithm (Wu et al. 2006) to optimize the percentage of on-time completion. This work improved the performance outcome of long-routing products, which is a crucial fault of the LBSA algorithm. However, batch-processing and machine instability were not considered in this work. These features may complicate the dispatching problem in a fab (Uzsoy et al. 1994).

There were some studies that focused on shop-floor control policies with TC issues. Lee and Jung (2003) proposed distributed shop-floor scheduling to decrease the rate of wafers exceeding TC. They found the optimal schedule, which met all targets and other constraints, where time constraints such as release times and deadlines are determined in advance through bidding-based production reservation. Wolfgang and Joerg (2000) developed a Kanban dispatching rule to reduce the influence of TC issues. To reduce the WIP level, they considered both machine breakdown and difference of arrival rates between each product. However, these studies did not consider the determination of batch size.

Summarizing the literature reviewed in this study, batch size determination is the key factor to conquering the TC issue in furnace operations. Moreover, a shop-floor control methodology should be involved to manage the WIP level within this stage.

3. DYNAMIC BATCH JOB CONTROL WITH TIME CONSTRAINTS (DBCTC)

The evidence shows that in order to resolve TC issues in the batch operations, the models for batch size determination and shop-floor control should be addressed. In this section, a Dynamic Batch Job Control with Time Constraints (DBCTC) is proposed. The batch size determination methodology, operation suspending/resuming rule, and job hold/release policy are all simultaneously involved in the proposed model. The system described in this work is the furnace operations of wafer fabrication, which is represented as Figure 1.

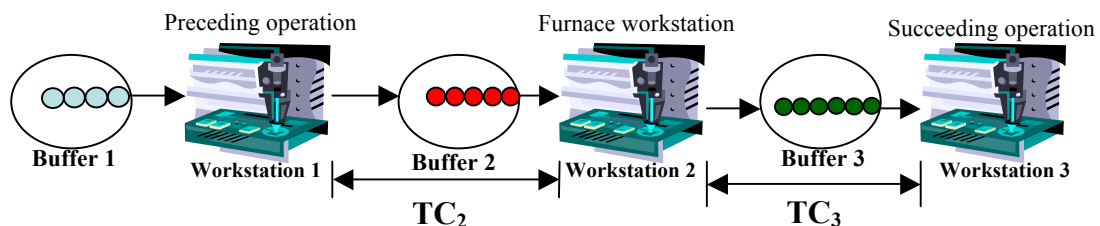


Figure 1. The furnace operations with TC

3.1 Notations

The following terms were required for the DBCTC.

m_i	Number of machines of workstation i
μ_i	Mean service rate of workstation i
B_i	Number of jobs in the queue at workstation i currently
TR_i	MTTR (Mean time to repair) of machine j at workstation i
A_i	Availability of workstation i
τ_i	Mean service time of workstation i
C_i	Maximum batch size (i.e. loading capacity) of workstation i
TC_i	Time length of TC at buffer i
PT	Processing time of current batch at furnace workstation
q_{ix}	Number of WIP of product x in the queue at workstation i
P	Number of product types processed in the system
W_{x1}	The weight of product x which has not exceeded TC
W_{x2}	The weight of product x which has exceeded TC

3.2 Safety WIP Level [S_i, s_i] of Workstations

The purpose of setting a maximum WIP level (S_i) in front of TC workstations (i.e. furnace workstation and its succeeding operation) is to prevent wafers from exceeding TC. Therefore, S_i should be the maximum number of customers that workstation i can service within the TC interval. The upstream operation should suspend its processing if the WIP level of workstation i is greater than S_i . Moreover, to prevent machine idle, the WIP level should be kept at a sufficient quantity to handle machine breakdown at the upstream operation. The equations are given below:

$$S_i = (TC_{i-1} \times m_i - \sum_{j=1}^{m_i} TR_{ij}) \times \mu_i \quad i=2,3 \quad \dots \quad (1)$$

$$s_2 = \sum_{j=1}^{m_1} TR_{j-1} \times \mu_2 \quad \dots \quad (2)$$

$$\mu_i = (1 / \tau_i) \times C_i \quad \dots \quad (3)$$

3.3 Minimum Batch Size of Furnace Workstation

To ensure that all jobs will leave the queue within the time window, a lowest service rate should be guaranteed. Hence, in the furnace workstation the minimum batch size (MB) should be addressed. Accordingly, the minimum batch size should be the current WIP level divided by the maximum number of batches that can be serviced within the TC interval. The equation is represented as follows.

$$MB = \frac{B_2}{(TC_2 / \tau_2) \times m_2} \quad \dots \quad (4)$$

3.4 Tolerance of Succeeding Operation

The tolerance of the succeeding operation (Tol) is defined as the maximum number of jobs that can be further increased in the buffer 3. Hence, Tol is the extra quantity of jobs that can be processed within the TC interval except what is already in buffer 3. The formula is represented as:

$$Tol = ((TC_2 \times m_3 - \sum_{j=1}^{m_3} TR_{3j}) \times \mu_i - B_3) - (\mu_2 \times m_2 - \mu_3 \times m_3) \quad \dots \quad (5)$$

3.5 Emergency Index of Product

The emergency index (I_x) is an index for product selecting to process at the furnace workstation. The I_x is the sum of reciprocals of remaining time to exceed TC, and of time length having already exceeded TC. There are two parts included in this index. The first one is the lots group under TC. In order to avoid exceeding TC, wafers closer to the TC boundary will have higher priority. The other group is the wafers having already exceeded TC. Because there is a negative correlation between waiting time and product yield, the wafers having just exceeded TC will be proposed to process first. Therefore, the emergency level is set as a negative correlation with the time of exceeding TC. Besides, a weighting (W_x) by product can be defined by managers. If the product is very important, the weight of this product can be set as a bigger number to increase its index value. The formula of emergency index is defined as follows.

$$I_x = W_{x1} \times \sum_{l=1, l \in S_1}^{N_{S1}} \left(\frac{1}{TC_2 - T_{xl}} \right) + W_{x2} \times \sum_{k=1, k \in S_2}^{N_{S2}} \left(\frac{1}{T_{xk} - TC_2} \right), \quad x = 1, \dots, P \quad \dots \quad (6)$$

Where,

T_{xl} is the waiting time of the l th lot remaining under TC

T_{xk} is the waiting time of the k th lot over TC

N_{S1} is the numbers of lot of product x under TC in the queue

N_{S2} is the numbers of lot of product x over TC in the queue

3.6 Shop-Floor Control Rule

I. Decision points.

The decisions should be made at the time of a lot's arrival or departure from the furnace workstation or its succeeding operation.

II. Decisions of suspending and reinstating proceeding operation (job hold/release)

- i. The proceeding operation should be suspended when B_2 is greater than S_2 or MB is greater than Tol .
- ii. When B_2 is smaller than S_2 , the proceeding operation should be reinstated.

III. Control rules for furnace workstation

- i. Selection of product. The product with largest emergency index should be selected into the workstation.
- ii. Determination of batch size. The batch size (Q) should be determined by following rule:

$$Q = \begin{cases} 0, & Tol < 0 \\ \text{Min}(C, Tol, q_{2,x}) & Tol \geq 0 \end{cases} \quad \dots \quad (7)$$

4. INDUSTRIAL APPLICATION AND SIMULATION EXPERIMENT

In this section, a numerical example is proposed and the effectiveness of the proposed model is validated. This example will demonstrate how the model set up and processed in the MES (Manufacturing Executing System). Furthermore, a series of simulation experiments were performed to compare the performances of the DBCTC, MBSX

and DJAH rules. Although TC issues are not considered by the MBSX and DJAH rules, the product yield would not be their major concern either. However, the MBSX and DJAH rules would be the most familiar dispatching rules in wafer fabrications. In comparing these two rules, the effectiveness of the DBCTC rule in wafer fabrications with TC issues can be confirmed.

4.1 Numerical Example

The example was designed to explore the characteristics of the furnace workstation and its preceding and succeeding operations. In the simulation model, the TCs were set in front of and in back of the furnace workstation. Wafers exceeding the TC set in front of the furnace operation will be reworked, but those exceeding the TC set in back of the furnace operation will be marked and continue their processes. There are three types of information in this example, including product mix, equipment and process data. The details are as the following tables.

Table 1. Monthly demand rate of products

<i>Product</i>	<i>Lots/month</i>	<i>Rate</i>
P1	960	0.1
P2	1920	0.2
P3	2880	0.3
P4	3840	0.4
Total	9600	1

Table 2. Detailed data of each workstation

	<i>Number of machines</i>	<i>Mean processing time (hr)</i>	<i>TC (hr)</i>	<i>MTTR (hr)</i>	<i>Availability</i>	<i>Maximum batch size</i>
Preceding operation	3	0.225	-	2	95%	1
Furnace workstation	8	3	9	4	95%	5
Succeeding operation	7	0.5264	4	2	95%	1

Table 3. Process data

<i>Workstation</i>	<i>Processing Time □ hr/batch □</i>	<i>Service Rate (lots/hr)</i>
Preceding operation	0.225	4.4444
Furnace workstation	3	1.6667
Succeeding operation	0.5264	1.8997

4.1.1 The Control of DBCTC module

The parameter of decisions of suspending and reinstating preceding operation (job hold/release) can be calculated as follows.

I. Maximum safety stock of Buffer₂ (S₂)

$$S_2 = (TC_2 \times m_2 - \sum_{j=1}^{m_2} TR_{2j}) \times \mu_2 = (9 \times 8 - 8 \times 4) \times 1.6667 = 66.668 \approx 67(\text{lots})$$

$$s_2 = \sum_{j=1}^{m_1} TR_{j-1} \times \mu_1 = (2 \times 3) \times 4.444 = 26.664 \approx 27(\text{lots})$$

$$S_3 = (TC_3 \times m_3 - \sum_{j=1}^{m_3} TR_{3j}) \times \mu_3 = (4 \times 7 - 7 \times 2) \times 1.8997 = 26.5958 \approx 27(\text{lots})$$

II. Tol and MB calculation

Assume the WIP amount in Buffer₂ is 30 lots and Buffer₃ is 20 lots. The value of Tol and MB can be calculated as below.

$$\begin{aligned} Tol &= ((TC_3 \times m_3 - \sum_{j=1}^{m_3} TR_{3j}) \times \mu_3 - B_3) - (\mu_2 \times m_2 - \mu_3 \times m_3) \times PT_2 \\ &= ((4 \times 7 - 7 \times 2) \times 1.8997 - 20) - (1.6667 \times 8 - 1.8998 \times 7) \times 1.6667 \\ &= 6.5375 \end{aligned}$$

$$MB = \frac{B_2}{(TC_2/PT_2) \times m_2} = \frac{50}{\frac{9}{1.6667} \times 8} = 1.1574$$

Due to $B_2 < S_2$, $Tol > MB$ and $B_3 < S_3$, the proceeding workstations and furnaces can process products continuously. The next step is to decide the lots should be processed in the furnace first. The emergency index of product (I_x) have to calculate.

III. The calculation of emergency index of product

Assume W_{x_1} is 1000 and W_{x_2} is 100 for all types of product. And the waiting time of lots in front of furnaces are as Table4.

Table 4. Lots information in Buffer₂

Lot	Product Type	Waiting Time	Lot	Product Type	Waiting Time
1	P1	0.5	16	P2	10
2	P1	0.5	17	P3	1
3	P1	1	18	P3	2
4	P1	2	19	P3	2
5	P1	5	20	P3	3
6	P1	8	21	P3	4
7	P1	9.5	22	P3	5
8	P1	10	23	P3	5
9	P2	1	24	P4	2
10	P2	1	25	P4	2
11	P2	3	26	P4	2.5
12	P2	3	27	P4	2.5
13	P2	3	28	P4	2.5
14	P2	4	29	P4	3
15	P2	9.5	30	P4	3

$$I_x = W_{x_1} \times \sum_{\substack{i=1 \\ i \in S_1}}^{N_{S_1}} \left(\frac{1}{TC_1 - T_{xi}} \right) + W_{x_2} \times \sum_{\substack{j=1 \\ j \in S_2}}^{N_{S_2}} \left(\frac{1}{T_{xj} - TC_1} \right) \quad x = 1, \dots, k$$

$$I_{p1} = 1000 \times \left(\frac{1}{9-0.5} + \frac{1}{9-0.5} + \frac{1}{9-1} + \frac{1}{9-2} + \frac{1}{9-5} + \frac{1}{9-8} \right) + 100 \times \left(\frac{1}{9.5-9} + \frac{1}{10-9} \right) = 2053.2$$

$$I_{p2} = 1250, \quad I_{p3} = 1277.4 \quad \text{and} \quad I_{p4} = 1080.6$$

Based on the calculation results, the emergency index of P1 is the largest. Therefore, P1 is selected to process in the furnace.

III. The decision of batch size

$$Q = \begin{cases} 0 & \text{Tol} < 0 \\ \text{Min}(C, \text{Tol}, q_{2,p1}) & \text{Tol} \geq 0 \end{cases}$$

$$Q = \text{Min}(5, 6.5375, 8) = 5$$

The batch size will be 5 lots and the final instruction is to select the lots of P1 product, lot3, 4, 5, 6, 7, 8 for furnace operation.

4.2 Simulation Experiment

In order to validate the effectiveness of the proposed model, a simulation experiment is performed. The data in this experiment is the same as the above example. Furthermore, the simulation program used in this work was eM-Plant version 7.0. The running horizon for each simulation was set at 360 days, 24 hours a day. The first 30 days comprised a warm-up period; therefore, the results are for the remaining 330 days. Each treatment was run 30 times to obtain average results. The following figure is the screen of this model in eM-Plant.

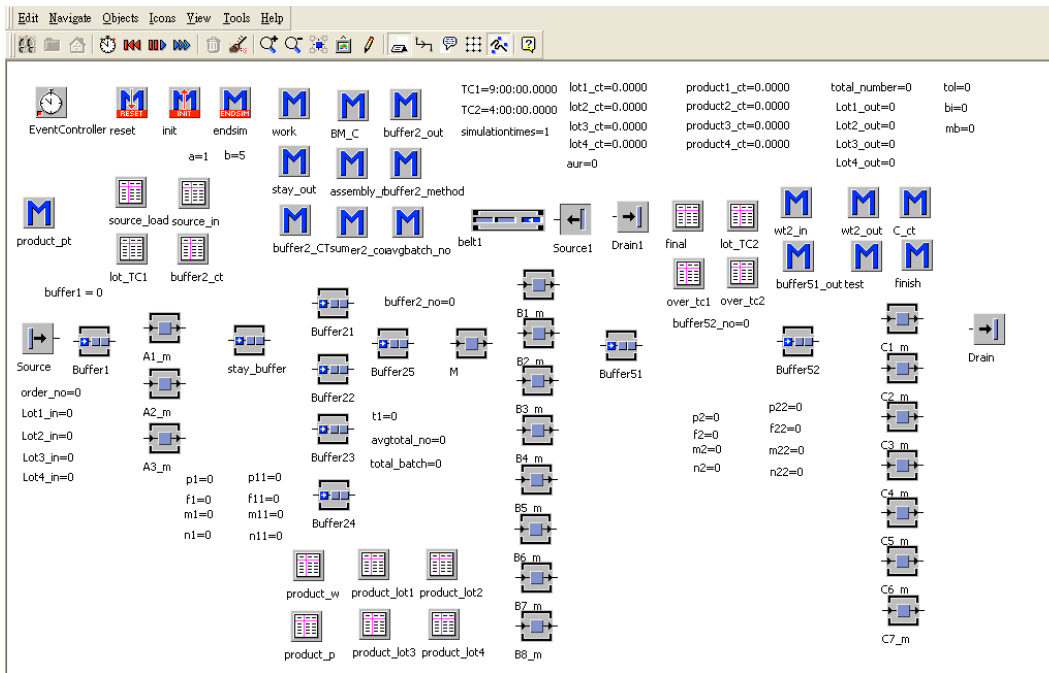


Figure 2. Simulation model

4.2.1 Determination of the Threshold of MBSX Rule

The first phase of the simulation experiment determines which threshold could get the best system performance with the MBSX rule. Comparing it with the best performances by the other rules can validate the proposed model more clearly. The maximum batch size (i.e. machine capability) of the furnace workstation is five; therefore, the threshold of the MBSX rule can be set from two to five. The comparison of different thresholds of the MBSX rule is represented in the following figures.

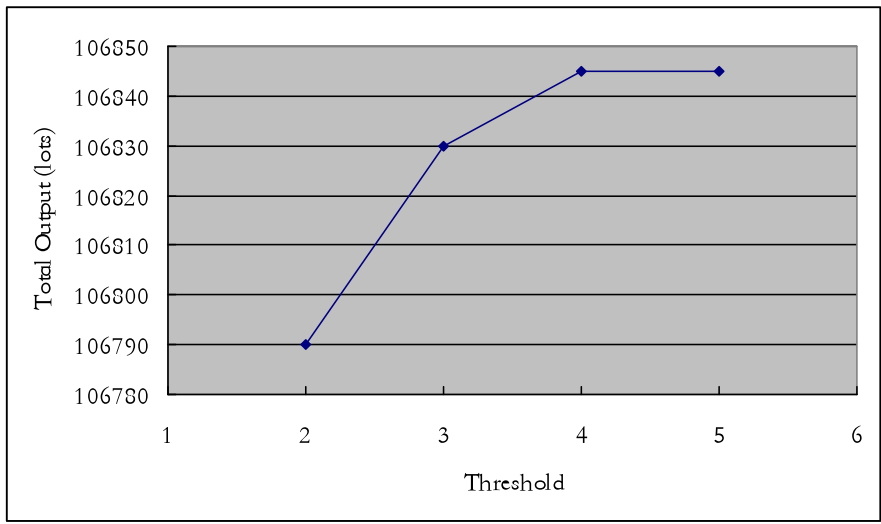


Figure 3. The comparison of total output between different thresholds in MBSX rule

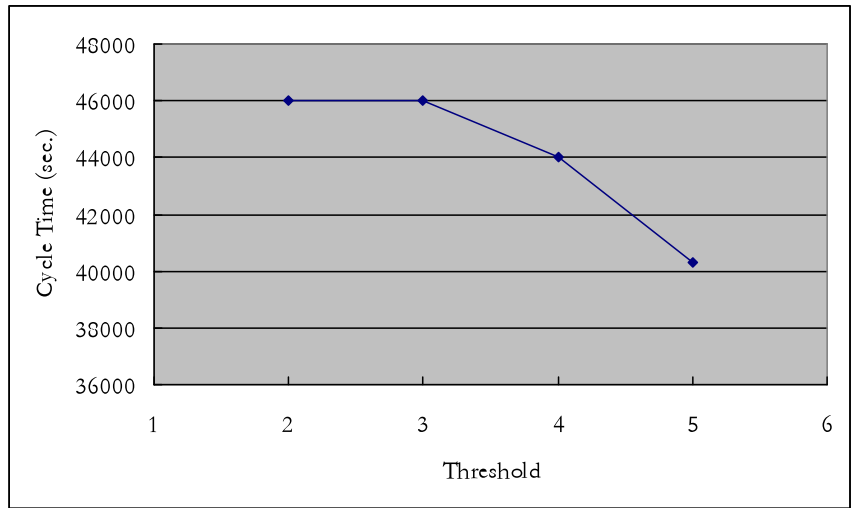


Figure 4. The comparison of average product cycle time between different thresholds in MBSX rule

From Figure 3 and Figure 4, the threshold (i.e. minimum batch size) set at five lots could produce the best system performances. In the following simulation experiment, therefore, the threshold of the MBSX rule is determined at five lots in order to be compared with the proposed model.

4.2.2 Performance Comparison between Different Models

In this section, the total output, defective output (output wafers exceeding TC) and average time length of exceeding TC of DBCTC, MBSX and DJAH were compared. Figures 5, 6, 7 and 8 present the results of comparison.

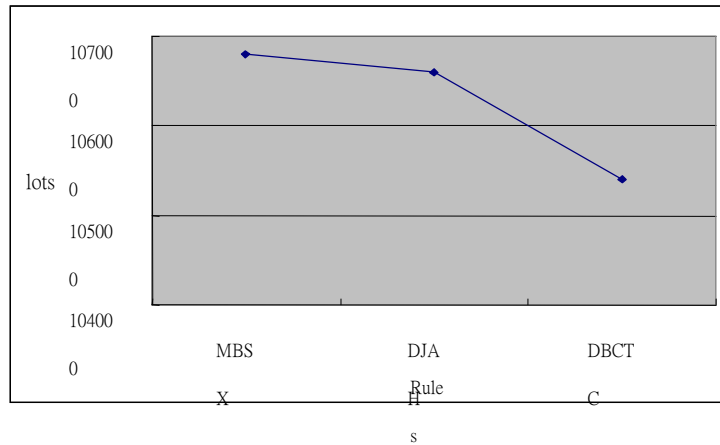


Figure 5. The comparison of total output of the system

Because the batch size of the furnace workstation is determined by the WIP level of the succeeding workstation in DBCTC model, more capacity could be lost in the proposed model. Thus the total output of the DBCTC may be less than that of the other two models. From Figure 5, the result shows that the output of DBCTC is lower than MBSX and DJAH indeed. However, the difference between the proposed model and the others is not significant (about 2%). Furthermore, the output of each rule includes wafers which exceeded TC, which may be scrapped in the Wafer Acceptance Test (WAT) stage. If only the effective output is considered, the performance of the proposed model will be better than the others.

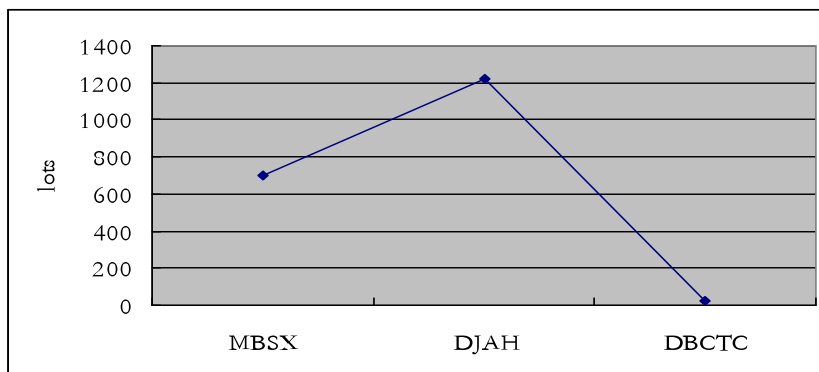


Figure 6. The comparison of quantity of wafers exceeded TC set in front of furnace workstation (lots)

Figure 6 represents the quantity of wafers that exceeded the TC set in front of the furnace workstation. Because the TC issues are not considered in the MBSX and DJAH rules, the quantities that exceeded TC for these two rules are far more than that of the DBCTC rule. Nevertheless, the quantities of wafers that exceeded TC in the MBSX

and DJAH rules are not very critical, while the processing logic of these two rules maximizes the utilization of the workstation. It means the logic of these two rules implies that WIP should be processed as soon as possible; the quantity of exceeded TC is controlled consequently.

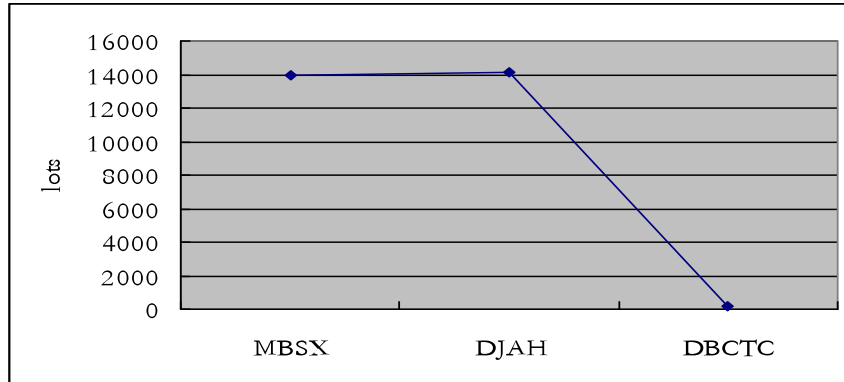


Figure 7. The comparison of quantity of wafers exceeded TC set in back of furnace workstation (lots)

From Figure 7, the quantities of wafers that exceeded the TC set in the succeeding operations of the furnace workstation are increased seriously in the MBSX and DJAH rules (over 10% of total output.) However, the DBCTC rule still gets a satisfying performance in this stage. To compare the result from Figure 6 and Figure 7, the phenomenon confirms that simply optimizing the furnace workstation will hurt the performance of the succeeding workstation, as stated above. Hence, the furnace workstation and succeeding process should be considered simultaneously to conquer the TC issues, especially in the succeeding workstation where it is more critical than the furnace operation in a foundry.

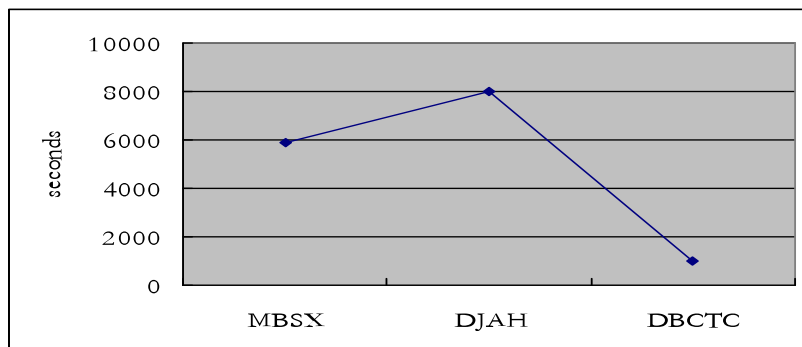


Figure 8. The comparison of average time length of exceeding TC

Furthermore, the average time length of exceeding TC is compared in Figure 8. The result proves that the proposed model gets better performance in not only quantity but also average time length of exceeding TC. The short time length of exceeding TC indicates that wafers will have more chance to pass the WAT test, even though the wafers have exceeded TC.

These figures supported that the proposed model could perform better in issues of TC with batch processing.

Although the DBCTC rule will perform a lower quantity of total output, it can get a more effective output than other rules. In the MBSX and DJAH rules, over 10% of total outputs have exceeded the TC set in front of and/or in back of the furnace workstation. Wafers exceeding TC will seriously affect the product yield; they even have to be scrapped eventually.

Moreover, the results indicated that we should consider the succeeding operation with TC in resolving TC issues at the furnace workstation. Maximizing output of the furnace workstation will also increase the loading of the succeeding operation. The objective of MBSX and DJAH is to optimize the furnace operation exclusively, therefore the performances of the succeeding operation became undesirable. The proposed model considered the furnace workstation and the succeeding operation simultaneously, and so could control the rate of wafers exceeding TC effectively.

5. CONCLUSIONS AND FUTURE WORK

In this work, a Dynamic Batch Job Control with Time Constraints (DBCTC) was proposed. By considering the furnace workstation and its succeeding operation simultaneously, the rate of wafers exceeding TC could be controlled effectively. Moreover, by adopting the concept of [S,s] policy, managers can suspend operation or decrease batch size dynamically to control the WIP at a safe level. The simulation experiments support that DBCTC could perform better than MBSX and DJAH in wafer fabrications with TC issues.

The setup time is another critical factor for batch size determination. The required time for machine setup will affect the result significantly. For instance, long setup time will result in a larger batch size to reduce setup times. Future studies should address setup time in the model.

6. ACKNOWLEDGEMENT

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7. REFERENCES

1. Cheraghi, S. H., Vishwaram, V. and Krishnan, K. K., 2003. Scheduling a single batch-processing machine with disagreeable ready times and due dates. *International Journal of Industrial Engineering: Theory, Applications and Practice*, **10**(2), 175-187.
2. Deb, R.K. and Serfozo, R.F., 1973. Optimal control of batch service queue. *Applied Probability*, **5**, 340-361.
3. Fowler, J.W., Philips, D.T. and Hogg, G.L., 1992. Real-time control of multi-product bulk-service semiconductor manufacturing process. *IEEE Transactions on Semiconductor Manufacturing*, **5**(2), 158-163.
4. Glassey, C.R. and Weng, W.W., 1991. Dynamic batching heuristic for simultaneous processing. *IEEE Transactions on Semiconductor Manufacturing*, **4**(2), 77-82.
5. Ikura, Y. and Gimple, M., 1986. Efficient Scheduling Algorithm for Single Batch Processing Machine. *Operation Research Letters*, **5**(2), 61-65.
6. Lee, S.H. and Jung, M.Y., 2003. Timing constraints' optimization of reserved tasks in the distributed shop-floor scheduling. *International Journal of Production Research*, **41**(2), 397-410.
7. Neuts, J.D.C., 1967. A general class of bulk queues with poisson input. *Annals of Mathematical statistics*, **38**,

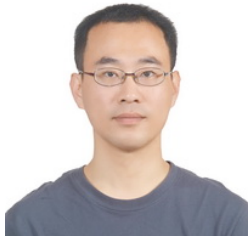
759-770.

8. Robinson, J. K. and Giglio, R., 1999. Capacity planning for semiconductor wafer fabrication with time constraints between operations. *Proceedings of 1999 Winter Simulation Conference*, **1**, 880-887.
9. Rulken, H.J.A., Van Campen, E.J.J., Van Herk, J., and Rooda J.E., 1998. Batch size optimization of furnace and pre-clean area by using dynamic simulations. *IEEE/SEMI Advanced Semiconductor Manufacturing Conference*, 439-444.
10. Tu, Y.M., and Chen, C.L., 2006. "The Influence of Arrival Smoothing between Batch and Serial Processes on System Performance," *The 7th Asia Pacific Industrial Engineering and Management Systems Conference*, Bangkok, Thailand, 1919-1924.
11. Tu, Y.M. and Liou, C.S., 2006. Capacity determination model with time constraints and batch processing in semiconductor wafer fabrication. *Journal of the Chinese Institute of Industrial Engineers*, **23**(3), 192-199.
12. Uzsoy, R., Louis, A.M. and Lee, C.Y., 1994. A Review of Production Planning and Scheduling Models in the Semiconductor Industry Part II: Shop-Floor Control. *IIE Transactions* **26**(5), 44-55.
13. Zee, D.J. van der; Harten, A. van; Schuur, P.C., 1997. Dynamic Job Assignment Heuristics for Multi-server Batch Operations — A Cost Based Approach. *International Journal of Production Research*, **35**(11), 3063-3093.
14. Wolfgang, S. and Joerg, D., 2000. Implementation of modeling and simulation in semiconductor wafer fabrication with time constraints between wet etch and furnace operations. *IEEE Transactions on Semiconductor Manufacturing*, **13**(3), 273-277.
15. Weng, W.W. and Leachman R.C., 1993. An improved methodology for real-time production decisions at batch-process work station. *IEEE Transactions on Semiconductor Manufacturing*, **6**(3), 219-225.
16. Wu, M.C. and Hung, T.U., 2008. A Hit-Rate Based Dispatching Rule for Semiconductor Manufacturing, *International Journal of Industrial Engineering: Theory, Applications and Practice*, **15**(1), 73-82.
17. Wu, M.C., Huang Y.L., Chang, Y.C. and Yang K.F., 2006. Dispatching in semiconductor fabs with machine-dedication features. *The International Journal of Advanced Manufacturing Technology*, **28**(9), 978-984.

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