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Learning before Erring: A Brief Note on the Influence of Dielectric Materials to pursue Moore's Law

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The semiconductor industry's ambitious scaling trends provide important guidelines for development by integrating knowledge from the past to self-correct its course. This paper illustrates said phenomenon by investigating the recent crises of static power losses in transistor structures. The impact of the power leaked through a device's drain has led to a drastic change in dielectric materials used, where silicon dioxide (SiO_2) insulators have been replaced with novel high-*k* dielectric constant materials. Yet, quantifiable evidence, which has recently emerged within research, suggests that even these new materials may not be sufficient enough to continue the scaling trajectory expected of Moore's Law, especially for low-powered devices. Based on industrial learning achieved from past trends, data collected for new dielectric materials, such as hafnium dioxide (HfO_2), and implied device scaling using Moore's Law, analysis suggests that current stand-by leakage limits will be breached in the near future.

Significance: The semiconductor industry's ability to learn and adapt to consumer product demands is crucial in order to reap the benefits implied by Moore's Law. This feat has been increasingly difficult to achieve for a variety of manufacturing and economical reasons. However, new high-*k* dielectric materials, such La_2O_3, have been employed to lower leakage current density below permissible levels. Thus, dielectric engineering will increase in significance for the final phases of Moore's Scaling Law.

Keywords: Moore's Law, gate leakage current density, high-*k* dielectric material, low-powered devices

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1. INTRODUCTION

Justifiably, many researchers have indicated that Moore's Law will not be sustained forever (Tummala, 2006). Research indicates emerging devices in the electronics industry, such as single electron tunneling devices, tunneling diodes, molecular nanoelectronics, spin devices, and wave interference devices, may eventually replace the dominant metal-oxide-semiconductor field effect transistors (MOSFET) device architecture (DeBenedictis, 2004). Yet, the silicon industry's persistent push for advancements in material and processing technologies, especially in the last decade, has extended Moore's scaling down to the sub-65 nanometer (nm) device architectures (Birnbaum & Williams, 2000). In the meantime, fundamental limitations in device physics are being pushed by the manufacturers while overall power dissipation and densities are becoming a real concern. Why? Because despite the many benefits that are obtained by reducing transistor sizes and operating voltages, downscaling leads to higher leakage currents due to extremely thin insulating layers and higher electric fields found inside MOSFETs. Thus, the more transistors on a chip equates to more power being wasted, which results in elevated operating temperatures that reduce chip performances and require more advanced cooling systems that can quickly drain a portable device's limited battery capacity.

This paper introduces the power dissipation problem, indicates its connection with static current leakage in devices, and explains how the intense work in the last decade resulted in high dielectric constant materials, such as HFO_2, which suppresses undesirable leakage effects. After analyzing the established scaling trends and the available gate leakage data, the results of this research demonstrate that the proposed (short-term) solutions for the gate leakage problem will need to be

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revisited by dielectric engineers in the near future. In terms of a design implication, HFO_2 will need to be replaced by alternative materials such as ZrO_2 and La_2O_3, which have higher dielectric constants.

2. PROBLEM BACKGROUND

Many in the semiconductor industry have stated that energy dissipation of electronic designs is the limiting factor for further scaling, especially given today's device speeds and chip densities (Kim, Austin, Mudge, Flautner, & Hu, 2003). There are two forms of power dissipation found in CMOS circuits. The *dynamic power* is associated to the power dissipated when logic gates in the integrated circuit charges and discharges its output capacitance during switching. Efficient circuit engineering and logic design is the only way to minimize this form of power loss. The *static* component of the transistor's power is the dissipation of power through the circuit when the transistor is in its "off-state," or holding logical states between switching events. Static power loss, although unavoidable, must be minimized because it does not contribute to logical computations.

The general objective in scaling microprocessors architecture is to concurrently reduce, supply voltage, gate threshold voltage, gate length, and oxide thickness, while keeping a sufficient drive current for the circuit (Frank, 2002). Scaling these design parameters in battery dependent portable systems is a considerable design challenge because smaller feature sizes lead to exponentially rising static leakage currents as device dimensions are reduced and internal electric fields rise. In addition, other leakage mechanisms, which were not a concern before, such as quantum mechanical tunneling, become active in insulators with a thickness in nanometer scale. Hence, the static power drained by these leakage mechanisms may be comparable to the dynamic power in poorly scaled devices or when the MOSFET gate length is reduced below 100nm as found in most advanced microchips today. Therefore, pursuing Moore's Law has become seriously challenging as more power may be consumed in the devices "off-state" rather than when the chips are actually being used to perform logical computations.

In order to reduce static and overall power dissipation and to continue the trajectory of Moore's Law, scientists are now researching both conventional and unconventional technologies (Hiremane, 2005). These include innovations in material, design, and packing as well as system-level design. Examples of these process-level innovations include experimenting with strained silicon, high dielectric constant (high-*k*) materials, and multi-gate transistors. At the architectural level, new approaches that enhance performance per logic instruction include the use of multi-core processors and super-pipelined architectures. However, among all alternatives, most significant gains are obtained by reducing the gate-oxide tunneling effect, which constitutes a large portion of static leakage below 100nm gate length. Said reduction can be achieved with the use of high-*k* dielectrics, which can increase the physical thickness of the insulating layer while still efficiently coupling the gate and channel charge. A projection of the impact of high-*k* dielectrics is shown in Figure 1 was adapted from Kim et al. (2003). This figure indicates that static power drained by the gate-oxide leakage could possibly be reduced if high-*k* dielectric materials were used in production. Yet, without the change to high-*k* dielectric materials, dynamic power consumption will be overtaken by static power consumption, making the trajectory of Moore's Law impractical to follow.

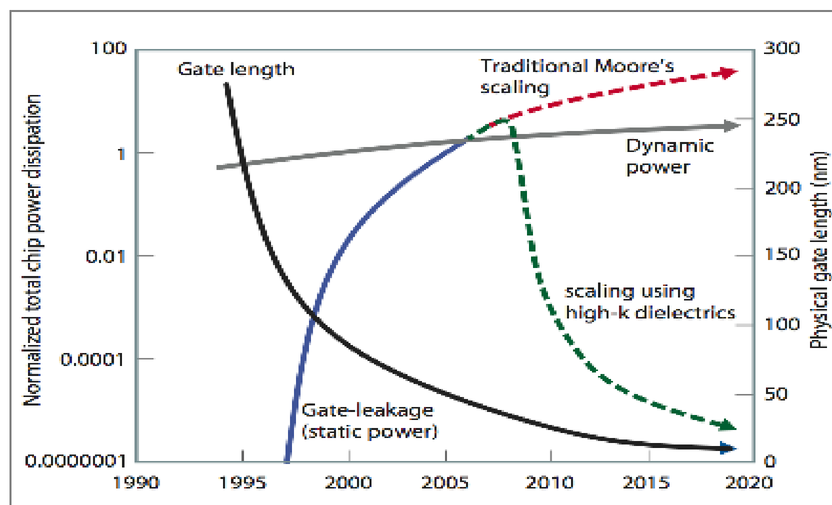

Figure 1. Total Chip Dynamic and Static Power Dissipation Trends

The exponential increase in power consumption of microprocessors is not only limited to the computer industry. A study from the Center for Power Electronics Systems stated forty percent of the total energy consumed in the United States was electrical energy (The Virginia Tech Research Division, 2002). Fifteen percent of this consumption was utilized by computer systems alone. Therefore, it is important to reduce power consumption not only for portable systems, but also for high-performance desktop systems that contribute significantly to this consumption (i.e. the economy). Moreover, there are also practical reasons why power consumption must be efficiently managed.

Figure 2 is an adaptation from Feng (2003), Kim (2005) Lundstrom (2006), and (CPU Scorecard, 2007) that shows the trajectory of microprocessor power dissipation in watts per cubic centimeters against year. For many years, power-density was rising with a steady trend towards the same levels as the Sun's surface (solid line). This trend, which is highly impractical, is several orders higher in magnitude than conventional air-cooling limitations. Although the main contribution to this power density had been the dynamic power dissipated during logic switching, in sub-100nm regime, the static leakage would exacerbate the power management problem.

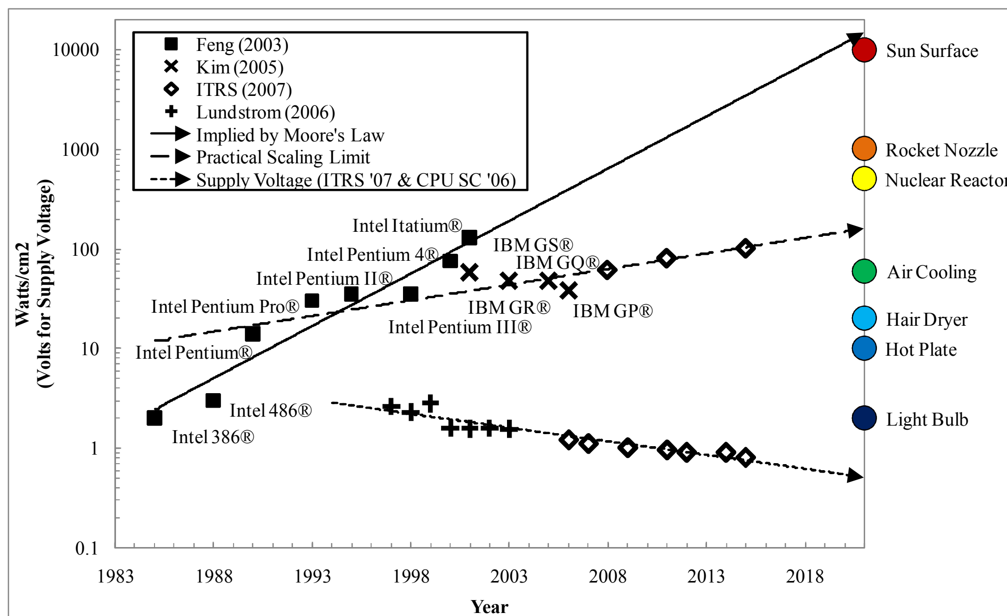

Figure 2. Logarithmic Power Consumption

The new power-scaling trend shown in Figure 2 as a heavy-dashed line was established in the year 2000. This paradigm change is a reflection of the use of first generation high-*k* dielectrics used in manufacturing such as oxynitrides (SiO_xN), which provides a small but easy-to-implement increase in dielectric constant. The scale of supply voltage is also shown in Figure 2 as thin-dashed line. The deceleration of supply voltage scaling is another very important design criterion for manufacturers. Despite efforts, power densities in silicon technologies have increased, thus there is a premium placed on the development of energy saving techniques rather than using costly fluid cooling approaches.

2.1 Objectives

The objective of this report is to emphasize the new "power-aware" scaling trends in silicon technology and examine if static power dissipation in MOSFET devices with high-*k* dielectric insulators can be reduced below the expected power limits in the final stretch of Moore's scaling below 45nm. The proposed examination will be based on the newly established scaling trends and ongoing research found in the field of dielectric material engineering. This research is significant because most non-specialists believe that the problems of static power dissipation have been resolved by using newly developed high-*k* dielectric materials such as HFO_2, which has been widely adopted in 45nm devices being shipped in 2008 (Intel, 2008). However, it will argue a need for re-visiting this issue in the near future by using quantifiable evidence found in literature and the implied rates of power scaling. It is concluded that static-power management and dielectric material engineering will remain an important aspect of scaling in the final decade of Moore's Law. At the same time, the study illustrates another example of how a semiconductor learns from past trends and adapts new solutions when faced with complex challenges such as power management, and has implications for material engineering as well as, system and consumer product design.

3. METHODOLOGY

Driven by economic realities, such as lower cost per transistor or logic operation, scaling CMOS device technology is a process that involves many facets of material science and engineering. Historically, semiconductor devices increase operating frequency by scaling down gate lengths, supply voltage, and equivalent oxide thickness to improve on-current drive, while maintaining off-current levels. Often, these trends are graphed in semi-logarithmic plots that show exponential trends. For example, the trend of equivalent oxide thickness (EOT, i.e. layer thickness normalized with respect to SiO_2 – the traditional insulator with a relative dielectric constant of ~3.9) is shown in Figure 3.

Historic data (Taur & Taur Ning, 1998) (ITRS, 2008) can be fitted with an exponential trend (dashed line), which has changed its slope (solid line) in the new era of dielectric engineering that has been the main approach to curb increasing static gate leakage problems. High-k insulators have been utilized to relax minimum thickness requirements for more effective gate coupling, which is responsible for deceleration reported by ITRS. This new trend is expected to continue until the end of practical scaling (~2020) at an EOT of 0.8nm.

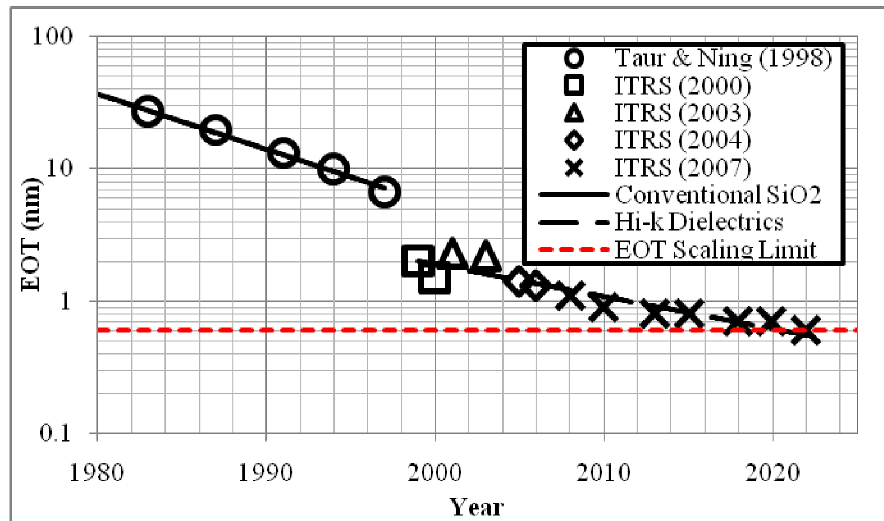

Figure 3. Historic and Future EOT Trends

As EOT scales down in size, the amount of leakage current density increases regardless of the dielectric material that is used. The thickness of gate insulator is the most important factor for tunneling current responsible for static leakage. However, other parameters such as the forbidden band-gap size and effective mass of electrons in an insulator are also important when EOT approaches its practical limit (~0.8 in Figure 3) in 2020, making it necessary to explore alternative materials. Accordingly, there have been a large number of experimental studies in literature that have reported leakage dependencies of such novel dielectrics as SiON (oxynitrides), HFSiON (hafnium oxynitrides), HFO_2 (hafnium oxide), Al_2O_3 (alumina), ZrO_2 (zirconium oxide) or La_2O_3 (lanthanum oxide) as a function of EOT under similar biasing conditions. The references used for the data collected for the various high-*k* dielectric materials are cited in Table 1. These references are also shown in Figure 4, where each line represents the average trend observed by the collection of data points of each material. Quantifiable forecast can now be made using current experimental results.

According to the ITRS (2008), the schedule for introducing dielectric materials in semiconductor devices is shown in Table 1. This schedule is very important when making long-term forecasts of the static power problem, since each material has its unique leakage characteristics and no sufficient research exists of all materials, which will delay their adoption in fabrication.

The focus of this study was only to factor in this work low-performance (LP) MOSFET devices intended for portable electronics applications as opposed to devices optimized for high-performance (HP) desktop systems that do not use a battery and can afford to operate at higher leakage densities using more aggressive cooling strategies. The proposed methodology, however, is perfectly applicable to HP devices if needed. This would require an alternative version of Figure 3, since actual HP devices are engineered differently with a different set of oxide thickness and threshold voltages. The foundation of this approach is to create transition curves in order to assign values of EOT for any given year. The transition curves in Figure 3 need to be as accurate as possible, which was achieved by including widely accepted values in the semiconductor industry for the past figures and common expectations compiled by ITRS for the next decade.

Table 1. Dielectric Material Schedule

Dielectric Material	Year Introduced	Year Discontinued	Dielectric Research References
SiO_2	1960	2004	(Timp, 1998) (McIntyre, 2002) (Watanabe, Ikarashi, & Ito, 2003) (Robertson, 2006)
SiO_xN	2001	2007	(Watanabe, Ikarashi, & Ito, 2003) (Robertson, 2006) (Tan, 2007)
HfSiON	2006	2010	(Watanabe, Ikarashi, & Ito, 2003) (Rhines, 2005) (Tan, 2007) (Yoshidaa, et al., 2007)
Al_2O_3	2007	2011	(Gusev, et al., 2001) (Lee, 2004) (Shiino, 2007)
HfO_2	2008	2014	(Guo & Ma, 1998) (DeGendt, 2004) (Lee, 2004) (Saraswat, 2006)
ZrO_2	2012	2017	(McIntyre, 2002) (Lee, 2004) (Saraswat, 2006) (Shiino, 2007)
La_2O_3	2015	2020	(Guha, Cartier, Bojarczuk, Bruley, Gignac, & Karasinski, 2001) (Iwai, 2004) (Deleonibus, 2007)

4. DESIGN IMPLICATIONS

To establish a likely path of development for leakage management via dielectric engineering up to year 2020, both the expected EOT values found in Figure 3 and the current density characteristics found in Figure 4 were used. Figure 5 represents forecasted values of leakage current densities in LP devices for new dielectric materials after 2009. In order to generate leakage estimates, the dielectric material schedule found in Table 1 can serve as a starting point for each material. For the implied range of years, EOT data can be obtained from the new scaling trend in Figure 3. Finally, the leakage performance of each material can be projected into this range by applying the collected data in Figure 4. For the sake of comparison, all of the high-*k* dielectric materials were forecasted from 2009 to 2020.

In order to provide a practical context for comparison and expectations, Figure 5 also includes the ITRS projected power limits which are shown as red lines. The stand-by power limit in low-power devices (LOSP) is the most important limit, as it is established with battery limits in mind.

The practical overall power limit in LP and HP devices is also included for completeness in order to provide a sense of scale. Note that over the years, the maximum power limits have been relaxed (as evidenced by similar data from earlier versions of ITRS found in Figure 5), as dielectric engineering provided additional capabilities and confidence in scaling.

When applying Figure 5, it can be concluded that intermediate gate-dielectric options, such as SiO_xN and HfSiON stacks, have limited gains, and are incapable of keeping static leakage power below even the overall operating-power limit expected of LP devices. The performance of alumina is especially disappointing as it is a marginal improvement over the HfSiON stack; it does not provide any incentive for a remarkable material change in fabrication. These materials have stand-by-power leakages that are substantially higher than allowed limits, and therefore cannot be used in portable systems of the next decade.

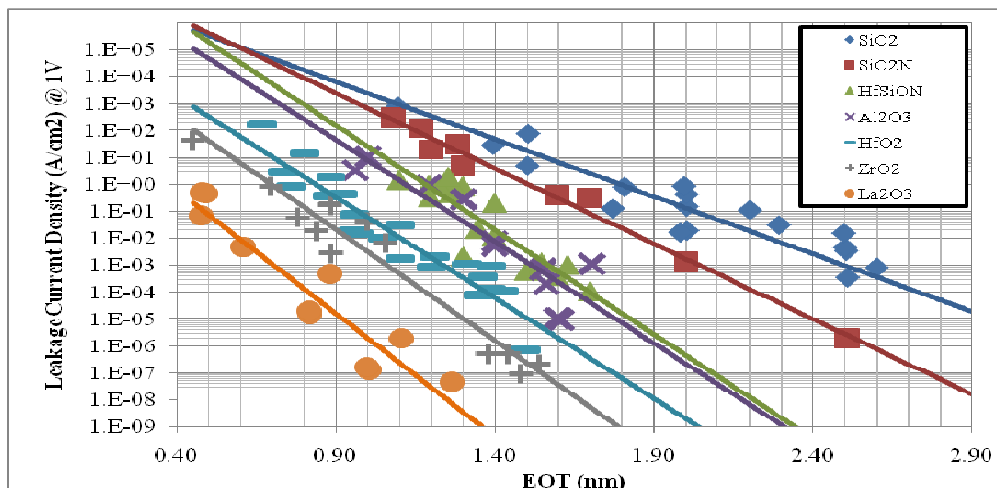

Figure 4. Dielectric Material Leakage Current Density

Most importantly, even with the relaxation of power limits (i.e. the small upward slope of red lines in Figure 5); it appears that even HfO_2 does not possess sufficient characteristics needed to curb static leakage beyond 2013. Although HfO_2 satisfies the LP operating limit (dashed red line in Figure 5), its inability to prevent leakage will be an issue for battery-operated systems and for frequency performance. This is because the excessive static leakage can only be tolerated with a compromise in operating frequency (i.e. dynamic power). ZrO_2 characteristics appear to be similar except that the lower leakage of this material is likely to extend its use until 2017. The material that offers the greatest advantage in terms of minimizing static leakage is La_2O_3. Clearly, La_2O_3 has a remarkable advantage over other high-*k* dielectrics that can last until the very end of Moore's traditional scaling of silicon systems, without penalties for battery or operating frequency.

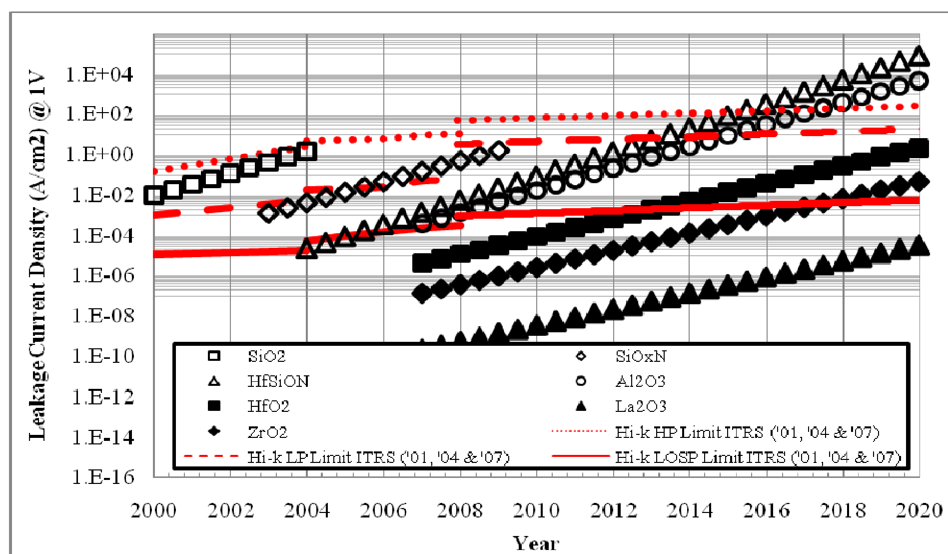

Figure 5. EOT Forecasted Leakage Current Density for Low Powered Devices

The analysis and estimates shown above could be considered inaccurate for a number of reasons. It was assumed that the above dielectrics could be integrated into planar Si MOSFET architecture without reduction in mobility, which would be counterproductive. This assumption is reasonable since an advanced understanding of interface structures and growth chemistry also helped resolve the mobility problems experienced initially with HfO_2.With ongoing nanomaterials and a nanofabrication revolution, it is highly possible to expect that atomic-layer deposition techniques will provide the necessary advancements needed for handling exotic dielectrics such as La_2O_3.. Secondly, it was also assumed that supply voltage would not decrease below 0.8V in this study. Any reduction in supply voltage can be beneficial for devices in terms of static leakage and elongate the duration of usage for any insulator. Thirdly, there is also a possibility that planar MOSFET architectures may be abandoned in favor of newer and non-planar MOSFET options, such as FinFETs and nanowire

MOSFETs, or 3D stacking of chips, which would make the above estimates less accurate. However, even these novel architectures and approaches will utilize high-*k* dielectrics, and therefore should conform to similar power constraints. In fact, such approaches will result in even higher power density in chips, hence requiring more strict limits for stand-by current leakage and consuming the benefits of HfO_2 even faster than this study suggests. Therefore, regardless of exact date for switching from HfO_2 to a new gate insulator, this analysis shows that the dielectric engineering will remain as a central theme for Si scaling.

In summary, recent efforts in semiconductor device manufacturing used to control excessive power dissipation and static power losses have been outlined. This potentially overwhelming problem has been dealt with by using novel dielectric materials, such as HfO_2. By using the latest scaling trends for insulators and available experimental leakage data, the benefits of HfO_2 will be short-lived and other high-*k* dielectric materials will be needed by 2013. In other words, the dielectric engineering will remain the driving force needed to determine the extent of Si scaling in the years to come. Most importantly, the dielectric engineering and the related story of power management demonstrates that the semiconductor industry has a exceptional zeal to self-correct and continually improve, which will be used to push the scaling down to 10nm range in the next decade, especially with the aid of advanced high-*k* dielectric materials.

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BIOGRAPHICAL SKETCH

William Young is a doctoral candidate in the Integrated Engineering program at Ohio University. His dissertation is focused on developing a team-compatibility decision support system. To fund this project, Mr. Young received Ohio University's 2007 Student Enhancement Award, which promotes creative academic research. Mr. Young recently accepted a position as a NFS GK-12 Fellow for the Science Technology Enrichment of Appalachian Middle-schoolers (STEAM) project. William received his Master's (MSEE) and Bachelor's (BSEE) degrees in Electrical Engineering at Ohio in 2005 and 2002 respectively. As a master's student, Young worked on a preliminary design cost estimation project for General Electric Aircraft Engines and developed a methodology to model a parts' family learning rate. His primary research is focused on developing methods for decision support systems, which includes intelligent systems such as neural networks.

Savas Kaya graduated from Istanbul Technical University in 1992 with a BSc in Electronics and Communication Engineering, received M.Phil. Degree in 1994 from the University of Cambridge, U.K., and Ph.D. degree in 1998 from Imperial College of Science, Technology & Medicine, London, U.K., for his work on strained Si quantum wells on vicinal substrates. From 1998 to 2001, he was a Postdoctoral Researcher at the University of Glasgow, Scotland, U.K., carrying out research in transport and scaling in Si/SiGe MOSFETs, and fluctuation phenomena in decanano MOSFETs. He is currently an Associate Professor at the Russ College of Engineering at Ohio University, Athens, OH. He has served as Air Force Office of Scientific Research Summer Faculty Fellow in 2006 and 2007. He published over 30 journal papers and 45 conference proceedings. His other interests include nanoelectronic devices and circuits, TCAD, transport theory, nanostructures, process integration, ionic transport and biomolecular modeling in trans-membrane proteins. Dr. Kaya was a member of the organizing committee for IWCE'7, 2000, and IEEE Nanotech'6, 2006.

Gary Weckman was a faculty member at Texas A&M University-Kingsville for six years before joining the Ohio University faculty in 2002 as an associate professor in Industrial and Systems Engineering. He has also practiced industrial engineering for over 12 years with firms such as; General Electric Aircraft Engines, Kenner Products and The Trane Company. Dr. Weckman's primary research focus has been multidisciplinary applications utilizing knowledge extraction techniques with artificial neural networks. He has used ANNs to model complex systems such as large-scale telecommunication network reliability, ecological relationships, stock market behavior, and industrial process scheduling. In addition, his research includes industrial safety and health applications and is on the Advisory Board for the University of Cincinnati NIOSH Occupational Safety and Health Education and Research Center Pilot Research Project.